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Call for Papers
The Ninth Japanese FPGA/PLD Design Conference
Thursday, January 24 - Friday, January 25, 2002 (2 days)
Pacifico Yokohama, Yokohama, JAPAN

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CONFERENCE GOALS AND BACKGROUND

The Japanese FPGA/PLD Design Conference is held in conjunction with the Electronic Design and Solution Fair, which provides a forum to exchange ideas and promote research in the fields of device technology, design technology, EDA support tools and applications for FPGA/PLD.

At the ninth conference, we are planning to introduce more practical technological information and leading-edge technological trends in the areas of devices, designs, EDA tools, and applications for FPGA/PLD, with a particular emphasis on the FPGA/PLD in the 21st century. To make possible more intensive discussion on current studies and the emerging ideas, the number of papers at the paper presentation session and tutorial sessions will be expanded at this conference. For example subjects handled in these sessions will include FPGA/PLD devices enabling entirely new functions, developing System-on-Chip (SoC) using IP, new design methodologies for FPGA/PLD in the 21st century and cutting-edge applications for FPGA/PLD.

Papers on or related to system LSI design, development and applications are invited. Papers from industry on case studies of designs or applications are also most welcome. Please bear in mind that the official language for the conference will be Japanese, and English will be adopted as a supplement. We are looking forward to your papers.

AREAS OF INTEREST

Papers from the following areas are invited.

a) Device architectures
b) Circuit design technology (High speed I/O, High density Circuits, etc.)
c) CAD/DA technology
d) Development support technology with FPGA/PLD-compatible IP
e) Developing System-on-Chip using IP or VSI
f) Compiler technology for embedded systems
g) Emulation technology and rapid prototyping
h) Hardware/Software Co-design
i) Re-configurable computing
j) Usage of FPGA/PLD with embedded cores
k) Evolving hardware
l) Any application using FPGA/PLD
m) Other topics related to FPGA/PLD

SUBMISSION OF PAPERS

Please send six (6) copies of extended abstracts with the completed application form to the address below. Papers will be reviewed by the program committee for selection. In addition to technical contents, extended abstracts are expected to contain a presentation outline describing project background, goals, approaches, importance and originality. Extended abstracts may not exceed four (4) A4-size pages, including the title, figures and tables. Abstracts exceeding four (4) pages will not be accepted.

APPLICATION FORM

Fill in the application form with the title of the paper, name and affiliation of the author(s), abstract (about 100 words), and up to three (3) keywords, with the name, contact address and affiliation of the corresponding author, postal code and address, telephone number, FAX number, and E-mail address. Applications will be accepted by e-mail or post. Application forms (templates) can be obtained by contacting the address below.

PRESENTATION

Selected papers will have a chance to be published at the proceedings, either in article style or on OHP slides, as preferred by the author(s) of papers. In case the number of the accepted papers is high, some authors will be asked to present their contents as short papers.

AWARD

Excellent papers will be awarded based on votes from the audience. Winning authors will be awarded at the conference. Supplementary prizes will be also provided to winning authors. In addition, all presenters will receive a conference tutorial ticket for the free viewing of one session.

IMPORTANT NOTICE

Travel costs for attending the conference will not be reimbursed.

SUBMISSION OF PAPERS

Deadline for submission of abstracts:	Oct. 15, 2001
Notification of acceptance:	Nov. 23, 2001
Deadline for camera-ready papers:	Dec. 20, 2001

Please send abstracts/application forms and inquires to:

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ORGANIZERS, SUPPORT AND ASSISTANCE

Organizers:
Steering Committee of The Ninth Japanese FPGA/PLD Design Conference
Japan Electronics and Information Technology Industries Association (JEITA)

Cooperation:
Electronic Design Automation Consortium

Support (expected):
Ministry of International Trade and Industry, Japan
Embassy of the United States of America in Japan
U.S. Semiconductor Industry Association (SIA)
Distributors Association of Foreign Semiconductors (DAFS)

Assistance (expected):
Institute of Electronics, Information and Communication Engineers (IEICE)
Information Processing Society of Japan (ISPJ)
Japan Printed Circuit Association (JPCA)