◆ CALL FOR PAPERS ◆

10th FPGA/PLD Design Conference

PACIFICO YOKOHAMA, Kanagawa, Japan
Thursday, January 30 to Friday, January 31, 2003 (2 days)

The FPGA/PLD Design Conference, Japan's only conference taking up the theme of FPGA/PLD, is held in conjunction with the Electronic Design and Solution Fair (http://www.edsfair.com/e_index.html), which provides a forum to exchange ideas and promote research in the fields of device technology, design technology, EDA support tools and applications for FPGA/PLD.

At the Ninth Conference, held in 2001, three grand prizes and one special prize were awarded for excellent User Presentations. The results are outlined in Japanese in the 2001 Exhibition Report (http://www.edsfair.com/2002/report/).

This year, in addition to the usual User Presentation program, we are planning to add an emphasis on introducing design case studies, which comprise the main feature of the Conference, including presentations of practical applications and design know-how. To this end, we are inviting papers on topics listed below, as well as those about or related to system LSI design, development and applications. Please bear in mind that the Conference will be held primarily in Japanese, and that English-language materials will be provided only for reference purposes in some cases. We are looking forward to receiving papers in a wide variety of related fields.

◇ Theme: Case studies on design, development support, applied technologies and devices related to FPGA/PLD

- Killer applications using FPGA/PLD
- Applications using FPGA/PLD
- Circuit design technology (high-speed I/O, high-density circuits, etc.)
- CAD/DA technologies (usage of conventional and new CAD/DA technologies)
- Development support technologies with FPGA/PLD-compatible IP
- System-on-Chip (SoC) development using IP or VSI, and related development support technologies
- Usage of FPGA/PLD with embedded cores
- Emulation technologies and rapid prototyping
- Compiler technologies for embedded systems
- Reconfigurable computing
- Software/hardware design
- FPGA/PLD device architectures
- Evolving hardware
- Other topics related to FPGA/PLD

◇ Submitting Papers

Before sending your paper, please submit the application form by e-mail, followed by an abstract of your paper in accordance with the instructions below. Papers for presentation will be reviewed by the Program Committee for selection. After receiving a notification of acceptance, please submit the paper in camera-ready format. Deadlines for each step in this process are as follows:

Submission of applications:	**Oct. 1, 2002**
Submission of abstracts:	**Oct. 15, 2002**
Notification of acceptance:	**Nov. 15, 2002**
Deadline for camera-ready papers:	**Dec. 20, 2002**

Application Form

Fill in the application form with the title of the paper, name(s) and position(s) of the author(s), a brief outline (up to about 300 Japanese characters), and up to three keywords. Please also include contact information for the person submitting the application (name, address, telephone and fax numbers, and e-mail address). Applications will be accepted by e-mail.

Submission of Abstract

Send a detailed abstract with the completed application form to the address below. Papers will be reviewed by the Program Committee for selection. In addition to technical contents, extended abstracts are expected to contain a presentation outline describing the project background, goals, approaches, importance and originality. Extended abstracts may not exceed four (4) A4-size pages, including the title, figures and tables. Abstracts exceeding four (4) pages will not be accepted. Please send the abstract as a data file in PDF format. If a PDF file cannot be provided, please contact Mr. Hironaka at Hiroshima City University.

Paper in Camera-Ready Format

Selected papers will be presented either in a conventional format or in the form of a presentation (PowerPoint or OHP), according to the preference of the author(s). If a high number of papers are selected, some authors might be asked to present their contents as short papers.

◇ Prizes

As was the case in 2001, this year excellent papers will be recognized based on votes by both the Program Committee and the audience. Award-winning authors will receive prizes at the Conference. Supplementary prizes will also be provided to winning authors. In addition, all presenters will receive an FPGA/PLD Design Conference tutorial ticket for the free viewing of one session.

◇ Abstracts/Application Forms and Inquires

Please send application forms, abstracts and inquiries for further information to the following contact:

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◇ Organizers, Cooperation, Support and Assistance

Organizers
Steering Committee of the 10th FPGA/PLD Design Conference
Japan Electronics and Information Technology Industries Association (JEITA)

Cooperation
Electronic Design Automation Consortium (EDAC)

Support (expected)
Ministry of the Economy, Trade and Industry, Japan (METI)
Embassy of the United States of America in Japan
U.S. Semiconductor Industry Association (SIA)
Distributors Association of Foreign Semiconductors (DAFS)

Assistance (expected)
Institute of Electronics, Information and Communication Engineers (IEICE)
Information Processing Society of Japan (ISPJ)
Japan Printed Circuit Association (JPCA)