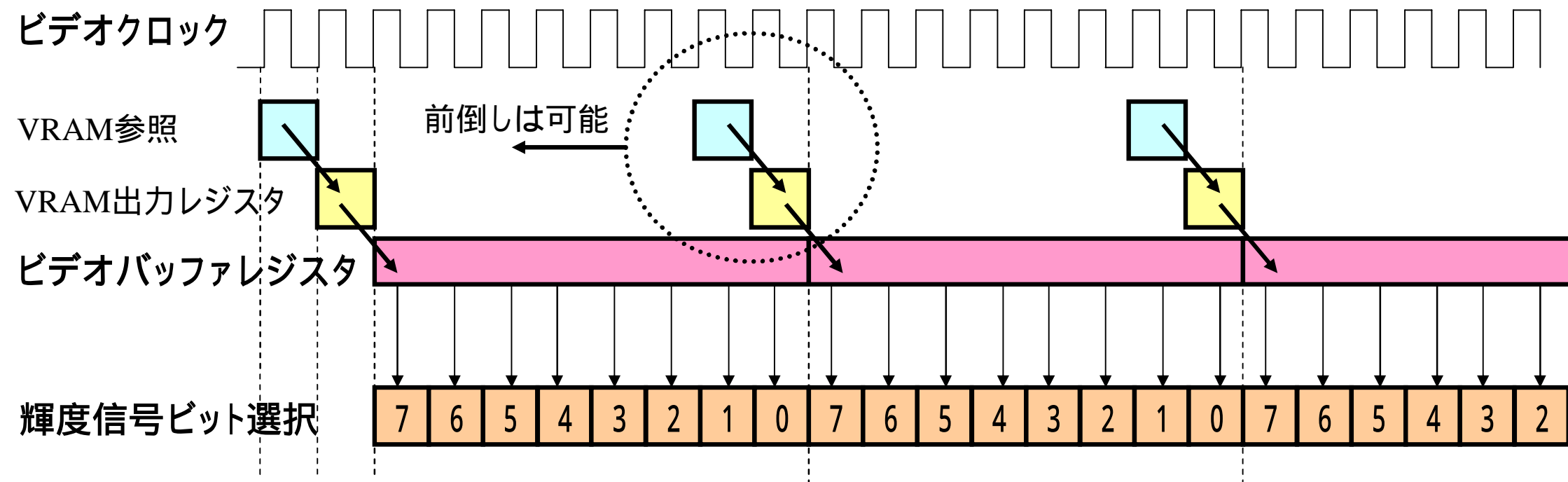


ビデオ周辺タイムチャート



輝度信号を駆動するビデオバッファはビデオクロックに同期
VRAM参照はバッファレジスタへ遅延なくデータを転送

X社FPGAへの合成

The screenshot displays the Xilinx Project Navigator interface. The left pane shows the project hierarchy for 'swsystem' on a 'xc3s200-4pq208' device. The main window shows the synthesis report for 'swsystem.syr'. The report includes a device utilization summary, a timing report, and clock information.

Device utilization summary:

Selected Device : 3s200pq208-4

Number of Slices:	1047	out of	1920	54%
Number of Slice Flip Flops:	383	out of	3840	9%
Number of 4 input LUTs:	1944	out of	3840	50%
Number of bonded IOBs:	10	out of	141	7%
Number of BRAMs:	3	out of	12	25%
Number of GCLKs:	2	out of	8	25%

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

Clock Signal	Clock buffer(FF name)	Load
div_clock:Q	BUFGP	385
clock	BUFGP	1

Timing Summary:

Speed Grade: -4

Minimum period: 37.892ns (Maximum Frequency: 26.391MHz)
Minimum input arrival time before clock: 7.079ns
Maximum output required time after clock: 8.391ns
Maximum combinational path delay: No path found