

ChipVision



- Company Location
 - Headquarters: Oldenburg, Germany
 - Representation in Japan: Innotech Corporation
- Company Profile
 - Leading provider of software tools & services to manage low-power estimation and implementation at the system level
- Products
 - Breakthrough ESL power optimization technology

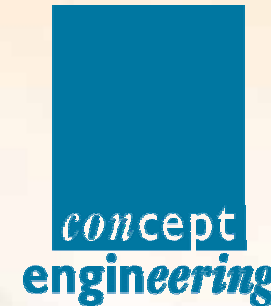
ChipVision



- Technology Key Features
 - Interactively creates power-optimized RTL code
- Key Benefits
 - Enables SOC architectural trade-offs for low-power
 - Reduces power up to 75% in power-critical blocks

Concept Engineering GmbH

- Company Location
 - Freiburg, Germany
- Company Profile
 - Concept's customizable debugging tools provide design engineers with the ability to quickly understand, debug and optimize their designs
- Product Names
 - SpiceVision PRO
 - GateVision PRO
 - RTLvision PRO



Concept Engineering GmbH

- Product Key Features
 - SpiceVision PRO
 - Transistor-level debugging (HSPICE, CDL, CALIBRE, ...)
 - RTLvision PRO
 - RTL-level debugging (VHDL, Verilog, SystemVerilog)
- Key Benefits
 - Supports pre- and post-layout transistor-level debugging (SpiceVision PRO)
 - Helps engineers to understand and integrate IP blocks (RTLvision PRO)

Entasys Design, Inc.

- Company Location
 - Seoul, Korea
- Company Profile
 - the leading provider of EDA solutions for ESL virtual prototyping
- Product Names
 - Pillar-DP-SOC

Entasys Design, Inc.

- Product Key Features
 - Pillar-DP-SOC
 - Power centric ESL virtual prototyping
- Key Benefits
 - Fast and accurate feasibility analysis
 - High performance estimation with what-if analysis
 - Unified solution for ESL virtual prototyping
 - Integrated solution for estimation and design planning

Javelin Design Automation



- Company Location
 - Silicon Valley, California, USA
- Leading Provider of SoC SPP
 - Specification-driven Physical Prototyping (SPP)
 - Delivering EARLY holistic and quality physical feedback
 - From architecture/ spreadsheet stage to Trial Netlists
- Javelin360 Enterprise Platform products
 - TrueFit Accurate Chip Estimation
 - TruePlan Pre-RTL and RTL Planning
 - TruePro Progressive SoC Prototyping

JavelinDesign Automation



- Javelin360 Key Features

- TrueFit

- Accurate Area-Content-Performance-Power-Process prediction and what-if tradeoff

- TruePlan and True Pro

- Area-Bus Interconnect Timing feasibility and optimization
- Prototype incomplete SoC and Blocks-in-context-of-chip during RTL development to optimize

- Key Benefits

- Cuts SoC Schedules and Project Costs by 35+%

- Minimize risk and iterations prior to Implementation (trial netlist)

- Achieves Higher-margin and QOS

- Pack content, performance and reduce power by efficient SoC design structure and FloorPlacement

Beach Solutions



- Company Location
 - San Jose, California, USA
- Company Profile
 - The leading provider of tools to manage SoC registers and auto-generate SoC design deliverables
- Product Names
 - EASI Core
 - EASI SoC
 - EASI Verification

Beach Solutions



- Product Key Features
 - EASI Core
 - Capture and manage IP address map
 - EASI SoC
 - Auto-generate interface design code
 - EASI Verification
 - Auto-generate integration tests and configuration files
- Key Benefits
 - Save SoC design time
 - Eliminates spec mis-communication