

## EDSFair2011 Nov. Exhibition Categories of Products to be Exhibited

<b>1 Hardware solutions</b>	Analizers
System LSI	Others
ASIC / ASSP	
MPU / MCU / DSP	
FPGA / PLD	
Others	
<b>2 Hardware development (EDA)</b>	
<b>i. IC design tools</b>	
System level design (higher than RTL)	
Logic design (RTL to net list)	
Logic verification	
Analog design / verification	
Physical implementation	
Physical verification / analysis	
Signal integrity analysis	
Test (DFT / BIST / ATPG / others)	
DFM (OPC / RET / PSM / LRC / CAD / others)	
ASIC Prototyping	
Others	
<b>ii. PCB / SIP design tools</b>	
Schematic capture	
Analog design / verification	
Layout	
Signal Integrity / Power Integrity / EMC analysis	
Electromagnetic field analysis	
Thermal analysis	
Others	
<b>3 Software solutions</b>	
Embedded OS	
Device drivers	
Firmware	
Middleware	
Virtual platform / Development	
Others	
<b>4 IC tester / analyzer</b>	
IC testers	
PCB testers	
<b>5 IP core, Macro, Cell libraries</b>	
<b>6 Embedded processor development environments</b>	
Reconfigurable processors	
ICE	
Debuggers	
Microcomputer CASE	
Compilers / Cross Compilers	
Simulators	
Hardware / Software co-design environments	
Others	
<b>7 Design service-related (LSI / PCB)</b>	
Design houses	
Design services	
Design consulting,	
Prototyping / Manufacturing	
IP distribution services	
Others	
<b>8 Design infrastructure (WS / PC, Network)</b>	
<b>9 Design data management tool</b>	
Design data management	
Others	
<b>10 Mask shop, Foundry</b>	
<b>11 University (R&amp;D), Consortium</b>	
<b>12 PR-related</b>	
Publications	
Others	

## Exhibitor Seminars Categories

\*may slightly change due to the number of applications

(A) ESL (including early SW development and virtual / HW prototyping)	(I) PCB
(B) Low Power	(J) SIP
(C) Timing convergence	(K) DFT
(D) DFM	(L) Physical verification
(E) Reliability (Power integrity)	(M) Physical implementation
(F) AMS design / verification	(N) Design / Verification service
(G) Functional verification (including HW prototyping)	(O) Thermal / Fluid analysis
(H) IP	(P) Others



electronic design and solution fair 2011 november

## Exhibition Application Form

### How to Apply

Please read the EDSFair 2011 Nov. Exhibition Regulations.

Fill in the required information on the application form, sign it and send it to the Show Management Office at (see below).

### Send to:

#### Japan Electronics Show Association

12F Ote Center Bldg., 1-1-3 Otemachi,  
Chiyoda-ku, Tokyo 100-0004, Japan  
TEL: 81-3-6212-5231 FAX: 81-3-6212-5225  
E-mail: info2011@edsfair.com

# November 16-18, 2011

Pacifico Yokohama, Japan

Sponsor: JEITA Japan Electronics and Information Technology Industries Association

## [www.edsfair.com/e/](http://www.edsfair.com/e/)

Concurrently held event : **Embedded Technology 2011**

# T0 Japan Electronics Show Association

Our company / organization will comply with all exhibition rules and regulations stipulated by both the Organizing Committee and Japan Electronics Show Association. In accordance with this agreement, we herewith submit the EDSFair 2011 Nov. Exhibition Application.



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## EDSFair 2011 Nov. Exhibition Application Form

Application deadline	Thursday, June 30, 2011
Date received	

### For official use only

Confirmation	Recipient No.	Member	Entry Date	Invoice	Booth No.

### Our company is a

Item marked with an asterisk (\*) must be filled in.

<input type="checkbox"/> Previous EDSFair exhibitor	<input type="checkbox"/> First-time exhibitor	(Please submit company profile and product catalogs.)
<input type="checkbox"/> Member of the Japan Electronics Show Association (JESA)	<input type="checkbox"/> Non-Member	

### Number of Booths applied for

Booth Configuration	Number applied for	Exhibition fee (tax included)	
<input type="checkbox"/> 1 row (1,2,3,4,5,6)	booth(s)	1 to 3 booth (s) @¥451,500 (General exhibitors fee) @¥399,000 (JESA member fee)	= ¥
<input type="checkbox"/> 2 rows (4,6,8,10,12)		4 or more booths @¥430,500 (General exhibitors fee) @¥378,000 (JESA member fee)	
<input type="checkbox"/> 3 rows (9,12,15,18)		Special fees for EDSFair2011Jan. exhibitors These special fees apply to only up to the same number of booth you exhibited at EDSFair2011 held in January. @¥294,000 (General exhibitors fee) @¥262,500 (JESA member fee)	
<input type="checkbox"/> 4 rows (16)			
<input type="checkbox"/> Block format (20,25,30,35,40,45,50)			
<input type="checkbox"/> Emerging Company Packaged Booth	booth(s)	@¥252,000	= ¥

### Exhibition Categories of Products to be Exhibited

Refer to Exhibition Categories of Products to be Exhibited on the reverse side and check all that apply to your product(s) to be exhibited.

<input type="checkbox"/> 1. Hardware solutions	<input type="checkbox"/> 5. IP core, Macro, Cell libraries	<input type="checkbox"/> 9. Design data management tool
<input type="checkbox"/> 2. Hardware development (EDA)	<input type="checkbox"/> 6. Embedded processor development environments	<input type="checkbox"/> 10. Mask shop, Foundry
<input type="checkbox"/> 3. Software solutions	<input type="checkbox"/> 7. Design service-related (LSI / PCB)	<input type="checkbox"/> 11. University (R&D), Consortium
<input type="checkbox"/> 4. IC tester / analyzer	<input type="checkbox"/> 8. Design infrastructure (WS / PC, Network)	<input type="checkbox"/> 12. PR-related

### Exhibitor Seminars

Refer to Exhibitor Seminars Categories on the reverse side and check the category to be expected with the number of applied sessions.

Fill the total number of applied sessions and the total usage fee in the blanks.

\*may slightly change due to the number of applications.

Categories	Number of sessions	Categories	Number of sessions
<input type="checkbox"/> A : ESL	sessions	<input type="checkbox"/> J : SIP	sessions
<input type="checkbox"/> B : Low Power	sessions	<input type="checkbox"/> K : DFT	sessions
<input type="checkbox"/> C : Timing convergence	sessions	<input type="checkbox"/> L : Physical verification	sessions
<input type="checkbox"/> D : DFM	sessions	<input type="checkbox"/> M : Physical implementation	sessions
<input type="checkbox"/> E : Reliability	sessions	<input type="checkbox"/> N : Design / Verification service	sessions
<input type="checkbox"/> F : AMS design / verification	sessions	<input type="checkbox"/> O : Thermal / Fluid analysis	sessions
<input type="checkbox"/> G : Functional verification	sessions	<input type="checkbox"/> P : Others	Please specify
<input type="checkbox"/> H : IP	sessions		
<input type="checkbox"/> I : PCB	sessions		
<b>Total</b>	sessions	@¥ 52,500	= (消費税込)

### Exhibitor Information

This information will appear in printed materials and on the official EDSFair website exactly as written, so please be careful to provide accurate information.

Please print using uppercase and lowercase letters, as appropriate.

Company Name (One letter per box, leave box empty for space)														
Head Office Information	Address													
	CEO'S Official Title							CEO'S Name						
Exhibition Supervisor	Address													
	Title / Division							Name						
	TEL							FAX						
	E-mail													
Invoice Address (Not necessary if same as above)	Address													
	Title / Division							Name						
	TEL							FAX						
	E-mail													
URL														

On behalf of my company, I hereby acknowledge that I have read, understood and will comply with the EDSFair 2011 Nov. Exhibition Regulations and herewith apply to exhibit.

Person in charge of our exhibit  
Company name:

Name (please print):

Job title:

Signature: