

EDSFair2013 Exhibition Categories of Products to be Exhibited

1 Hardware solutions

System LSI
ASIC / ASSP
MPU / MCU / DSP
FPGA / PLD
Others

2 Hardware development (EDA)

i. IC design tools

System level design (higher than RTL)
Logic design (RTL to net list)
Logic verification
Analog design / verification
Physical implementation
Physical verification / analysis
Signal integrity analysis
Test (DFT / BIST / ATPG / others)
DFM (OPC / RET / PSM / LRC / CAD / others)
ASIC Prototyping
Others

ii. PCB / SIP design tools

Schematic capture
Analog design / verification
Layout
Signal Integrity / Power Integrity / EMC analysis
Electromagnetic field analysis
Thermal analysis
Others

3 Software solutions

Embedded OS
Device drivers
Firmware
Middleware
Virtual platform / Development
Others

4 IC tester / analyzer

IC testers
PCB testers

Analyzers
Others

5 IP core, Macro, Cell libraries

6 Embedded processor development environments

Reconfigurable processors
ICE
Debuggers
Microcomputer CASE
Compilers / Cross Compilers
Simulators
Hardware / Software co-design environments
Others

7 Design service-related (LSI / PCB)

Design houses
Design services
Design consulting
Prototyping / Manufacturing
IP distribution services
Others

8 Design infrastructure (WS / PC, Network)

9 Design data management tool

Design data management
Others

10 Mask shop, Foundry

11 University (R&D), Consortium

12 PR-related

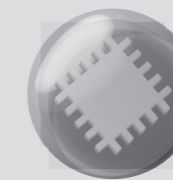
Publications
Others

Exhibitor Seminars Categories

*may slightly change due to the number of applications

(A) ESL (including early SW development and virtual / HW prototyping)
(B) Low Power
(C) Timing convergence
(D) DFM
(E) Reliability (Power integrity)
(F) AMS design / verification
(G) Functional verification (including HW prototyping)
(H) IP
(I) PCB

(J) SIP
(K) DFT
(L) Physical verification
(M) Physical implementation
(N) Logic design
(O) Design / Verification service
(P) Electromagnetic field / Thermal / Fluid analysis
(Q) FPGA-related
(R) Others



edsfair

electronic design and solution fair 2013

Exhibition Application Form

How to Apply

Please read the EDSFair2013 Exhibition Regulations.

Fill in the required information on the application form, sign it and send it to the Show Management Office at (see below).

Send to:

Japan Electronics Show Association

12F Ote Center Bldg., 1-1-3 Otemachi,
Chiyoda-ku, Tokyo 100-0004, Japan
TEL: 81-3-6212-5231 FAX:81-3-6212-5225
E-mail: info2013@edsfair.com

November 20-22, 2013

Pacifico Yokohama, Japan

Sponsor: JEITA Japan Electronics and Information Technology Industries Association

www.edsfair.com/e/

Concurrently held event : **Embedded Technology 2013**

T0 Japan Electronics Show Association

Our company / organization will comply with all exhibition rules and regulations stipulated by both the Organizing Committee and Japan Electronics Show Association. In accordance with this agreement, we herewith submit the EDSFair2013 Exhibition Application.



electronic design and solution fair 2013
Exhibition Application Form

Application deadline	Friday, June 28, 2013
Date received	

For official use only

Confirmation	Recipient No.	Member	Entry Date	Invoice	Booth No.

Our company is a

Item marked with an asterisk (*) must be filled in.

<input type="checkbox"/> Previous EDSFair exhibitor	<input type="checkbox"/> First-time exhibitor	(Please submit company profile and product catalogs.)
<input type="checkbox"/> Member of the Japan Electronics Show Association (JESA)	<input type="checkbox"/> Non-Member	

Number of Booths applied for

Booth Configuration	Number applied for	Exhibition fee (tax included)	
Standard Booth			
<input type="checkbox"/> 1 row (1,2,3,4,5,6)	booth(s)	1 to 3 booth (s) @¥451,500 (General exhibitors fee) @¥399,000 (JESA member fee)	= ¥
<input type="checkbox"/> 2 rows (4,6,8,10,12)			
<input type="checkbox"/> 3 rows (9,12,15,18)			
<input type="checkbox"/> 4 rows (16)			
<input type="checkbox"/> Block format (20,25,30,35,40,45,50)		4 or more booths @¥430,500 (General exhibitors fee) @¥378,000 (JESA member fee)	
<input type="checkbox"/> Small Packaged Booth (1,2)	booth(s)	@¥367,500	= ¥
<input type="checkbox"/> Emerging Company Packaged Booth (1,2,3)	booth(s)	@¥252,000	= ¥

Exhibition Categories of Products to be Exhibited

Refer to Exhibition Categories of Products to be Exhibited on the reverse side and check all that apply to your product(s) to be exhibited.

<input type="checkbox"/> 1. Hardware solutions	<input type="checkbox"/> 5. IP core, Macro, Cell libraries	<input type="checkbox"/> 9. Design data management tool
<input type="checkbox"/> 2. Hardware development (EDA)	<input type="checkbox"/> 6. Embedded processor development environments	<input type="checkbox"/> 10. Mask shop, Foundry
<input type="checkbox"/> 3. Software solutions	<input type="checkbox"/> 7. Design service-related (LSI / PCB)	<input type="checkbox"/> 11. University (R&D), Consortium
<input type="checkbox"/> 4. IC tester / analyzer	<input type="checkbox"/> 8. Design infrastructure (WS / PC, Network)	<input type="checkbox"/> 12. PR-related

Exhibitor Seminars

Refer to Exhibitor Seminars Categories on the reverse side and check the category to be expected with the number of applied sessions.

Fill the total number of applied sessions and the total usage fee in the blanks.

*may slightly change due to the number of applications.

Categories	Number of sessions	Categories	Number of sessions
<input type="checkbox"/> A : ESL	sessions	<input type="checkbox"/> K : DFT	sessions
<input type="checkbox"/> B : Low Power	sessions	<input type="checkbox"/> L : Physical verification	sessions
<input type="checkbox"/> C : Timing convergence	sessions	<input type="checkbox"/> M : Physical implementation	sessions
<input type="checkbox"/> D : DFM	sessions	<input type="checkbox"/> N : Logic design	sessions
<input type="checkbox"/> E : Reliability	sessions	<input type="checkbox"/> O : Design / Verification service	sessions
<input type="checkbox"/> F : AMS design / verification	sessions	<input type="checkbox"/> P : Electromagnetic field / Thermal / Fluid analysis	sessions
<input type="checkbox"/> G : Functional verification	sessions	<input type="checkbox"/> Q : FPGA-related	sessions
<input type="checkbox"/> H : IP	sessions	<input type="checkbox"/> R : Others	sessions
<input type="checkbox"/> I : PCB	sessions	Please specify (tax included)	
<input type="checkbox"/> J : SIP	sessions		
Total	sessions	@¥63,000	=¥

Suites

Type	Number of Suites	Room charge (tax included)	
S (3.96 m × 3.96 m)	Suite(s)	@¥367,500	=¥
M (5.94 m × 3.96 m)	Suite(s)	@¥441,000	=¥
L (5.94 m × 4.95 m)	Suite(s)	@¥504,000	=¥

Exhibitor Information

This information will appear in printed materials and on the official EDSFair website exactly as written, so please be careful to provide accurate information.

Please print using uppercase and lowercase letters, as appropriate.

Company Name (One letter per box, leave box empty for space)																
Head Office Information	Address															
	CEO'S Official Title											CEO'S Name				
Exhibition Supervisor	Address															
	Title / Division											Name				
	TEL											FAX				
	E-mail															
Invoice Address (Not necessary if same as above)	Address															
	Title / Division											Name				
	TEL											FAX				
	E-mail															
URL																

On behalf of my company, I hereby acknowledge that I have read, understood and will comply with the EDSFair2013 Exhibition Regulations and herewith apply to exhibit.

Person in charge of our exhibit
Company name: _____

Name (please print): _____

Job title: _____

Signature: _____