EDSFair2012 Exhibition Categories of Products to be Exhibited

1 Hardware solutions
- System LSI
- ASIC / ASSP
- MPU / MCU / DSP
- FPGA / PLD
- Others

2 Hardware development (EDA)

i. IC design tools
- System level design (higher than RTL)
- Logic design (RTL to net list)
- Logic verification
- Analog design / verification
- Physical implementation
- Physical verification / analysis
- Signal integrity analysis
- Test (DFT / BIST / ATPG / others)
- DFM (OPC / RET / PSM / LRC / CAD / others)
- ASIC Prototyping
- Others

ii. PCB / SIP design tools
- Schematic capture
- Analog design / verification
- Layout
- Signal Integrity / Power Integrity / EMC analysis
- Electromagnetic field analysis
- Thermal analysis
- Others

3 Software solutions
- Embedded OS
- Device drivers
- Firmware
- Middleware
- Virtual platform / Development
- Others

4 IC tester / analyzer
- IC testers
- PCB testers
- Analyzers
- Others

5 IP core, Macro, Cell libraries

6 Embedded processor development environments
- Reconfigurable processors
- ICE
- Debuggers
- Microcomputer CASE
- Compilers / Cross Compliers
- Simulators
- Hardware / Software co-design environments
- Others

7 Design service-related (LSI / PCB)
- Design houses
- Design services
- Design consulting
- Prototyping / Manufacturing
- IP distribution services
- Others

8 Design infrastructure (WS / PC, Network)

9 Design data management tool
- Design data management
- Others

10 Mask shop, Foundry

11 University (R&D), Consortium

12 PR-related
- Publications
- Others

Exhibitor Seminars Categories

*may slightly change due to the number of applications

- **(A) ESL** (including early SW development and virtual / HW prototyping)
- **(B) Low Power**
- **(C) Timing convergence**
- **(D) DFM**
- **(E) Reliability** (Power integrity)
- **(F) AMS design / verification**
- **(G) Functional verification** (including HW prototyping)
- **(H) IP**
- **(I) PCB**
- **(J) SIP**
- **(K) DFT**
- **(L) Physical verification**
- **(M) Physical implementation**
- **(N) Logic design**
- **(O) Design / Verification service**
- **(P) Electromagnetic field / Thermal / Fluid analysis**
- **(Q) FPGA-related**
- **(R) Others**

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electronic design and solution fair 2012

Exhibition Application Form

How to Apply

Please read the EDSFair2012 Exhibition Regulations.
Fill in the required information on the application form, sign it and send it to the Show Management Office at (see below).

Send to:

Japan Electronics Show Association

12F Ote Center Bldg., 1-1-3 Otemachi,
Chiyoda-ku, Tokyo 100-0004, Japan
TEL: 81-3-6212-5231 FAX:81-3-6212-5225
E-mail: info2012@edsfair.com

November 14-16, 2012

Pacifico Yokohama, Japan

Sponsor: JEITA Japan Electronics and Information Technology Industries Association

www.edsfair.com/e/

Concurrently held event : Embedded Technology 2012

TO Japan Electronics Show Association

Our company / organization will comply with all exhibition rules and regulations stipulated by both the Organizing Committee and Japan Electronics Show Association. In accordance with this agreement, we herewith submit the EDSFair2012 Exhibition Application.

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electronic design and solution fair 2012

EDSFair2012 Exhibition Application Form

Application deadline	**Friday, June 29, 2012**
Date received	

For official use only

Confirmation	Recipient No.	Member	Entry Date	Invoice	Booth No.

Our company is a

Item marked with an asterisk (※) must be filled in.

※
- ☐ Previous EDSFair exhibitor ☐ First-time exhibitor (Please submit company profile and product catalogs.)
- ☐ Member of the Japan Electronics Show Association (JESA) ☐ Non-Member

Number of Booths applied for

※

Booth Configuration	Number applied for	Exhibition fee (tax included)	
Standard Booth ☐ 1 row (1,2,3,4,5,6) ☐ 2 rows (4,6,8,10,12) ☐ 3 rows (9,12,15,18) ☐ 4 rows (16) ☐ Block format (20,25,30,35,40,45,50)	booth(s)	1 to 3 booth (s) @¥451,500 (General exhibitors fee) @¥399,000 (JESA member fee) 4 or more booths @¥430,500 (General exhibitors fee) @¥378,000 (JESA member fee)	= ¥
☐ Small Packaged Booth (1,2)	booth(s)	@¥367,500	= ¥
☐ Emarging Company Packaged Booth (1,2,3)	booth(s)	@¥252,000	= ¥

Exhibition Categories of Products to be Exhibited

Refer to Exhibition Categories of Products to be Exhibited on the reverse side and check all that apply to your product(s) to be exhibited.

※

☐ 1. Hardware solutions	☐ 5. IP core, Macro, Cell libraries	☐ 9. Design data management tool
☐ 2. Hardware development (EDA)	☐ 6. Embedded processor development environments	☐ 10. Mask shop, Foundry
☐ 3. Software solutions	☐ 7. Design service-related (LSI / PCB)	☐ 11. University (R&D), Consortium
☐ 4. IC tester / analyzer	☐ 8. Design infrastructure (WS / PC, Network)	☐ 12. PR-related

Exhibitor Seminars

Refer to Exhibitor Seminars Categories on the reverse side and check the category to be expected with the number of applied sessions.
Fill the total number of applied sessions and the total usage fee in the blanks.
＊may slightly change due to the number of applications.

Categories	Number of sessions	Categories	Number of sessions
☐ A : ESL	sessions	☐ K : DFT	sessions
☐ B : Low Power	sessions	☐ L : Physical verification	sessions
☐ C : Timing convergence	sessions	☐ M : Physical implementation	sessions
☐ D : DFM	sessions	☐ N : Logic design	sessions
☐ E : Reliability	sessions	☐ O : Design / Verification service	sessions
☐ F : AMS design / verification	sessions	☐ P : Electromagnetic field / Thermal / Fluid analysis	sessions
☐ G : Functional verification	sessions	☐ Q : FPGA-related	sessions
☐ H : IP	sessions	☐ R : Others	sessions
☐ I : PCB	sessions	Please specify	
☐ J : SIP	sessions		(tax included)
Total	sessions	@¥63,000	=¥

Suites

Type	Number of Suites	Room charge (tax included)	
S (3.96 m × 3.96 m)	Suite(s)	@¥367,500	=¥
M (5.94 m × 3.96 m)	Suite(s)	@¥441,000	=¥
L (5.94 m × 4.95 m)	Suite(s)	@¥504,000	=¥

Exhibitor Information

This information will appear in printed materials and on the official EDSFair website exactly as written, so please be careful to provide accurate information.
Please print using uppercase and lowercase letters, as appropriate.

※

Company Name (One letter per box, leave box empty for space)				
Head Office Information	Address			
	CEO'S Official Title		CEO'S Name	
Exhibition Supervisor	Address			
	Title / Division		Name	
	TEL		FAX	
	E-mail			
Invoice Address (Not necessary if same as above)	Address			
	Title / Division		Name	
	TEL		FAX	
	E-mail			
URL				

On behalf of my company, I hereby acknowledge that I have read, understood and will comply with the EDSFair2012 Exhibition Regulations and herewith apply to exhibit.

※
Person in charge of our exhibit
Company name:

Name (please print):

Job title:

Signature: